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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,993	09/20/2001	Yutaka Toyonoh	TI-33251 (032350.B343)	9873

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,993	TOYONOH ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-12 and 17-20* is/are rejected.

7)☒ Claim(s) *4-7 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are examined.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because of the following informalities: the applicant is advised to remove underline the title in specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 8-12, and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art.

Re claim 1, the admitted prior art discloses in Figure 1 of the present application a Booth encoding circuit (100) comprising: a plurality of cells (e.g. 102a, 102b excluding an inverter, 102c including the inverter, and 102d), wherein at least one of cells (e.g. 102c with the inverter) comprises: a plurality of inputs (Y_{2n}, Y_{2n-1}, and Y_{2n+1}); a first plurality of transistors (110a-110d) forming a first logic stage, wherein at least one of inputs (Y_{2n-1}) is connected to at least one of first plurality of transistors; a second plurality of transistors (110e-110h) forming a second logic stage, wherein at least one of inputs (Y_{2n-1}) is connected to at least one of second plurality of transistors; a first output inverter (the inverter in 102b) connected to at least one of second plurality of transistors (110e); a first switching means (103a) connected to at least one of first plurality of transistors; a second switching means (103b) connected to first output inverter; a second output inverter (the

inverter that connect to 103ab) connected to first switching means (103a) and second switching means (103b), wherein within a critical path of Booth encoding circuit first output inverter drives second output inverter (through 103b).

Re claim 2, the admitted prior art further discloses in Figure 1 of the present application critical path of Booth encoding circuit first output inverter drives second output inverter via second switching means (the connection signal from inverter 102b drive the switch 103b which connects to the 2nd inverter in 102c).

Re claim 3, the admitted prior art further discloses in Figure 1 of the present application first switching means comprises a first transfer gate switch (103a) and second switching means comprise a second transfer gate switch (103b).

Re claim 8, the admitted prior art further discloses in Figure 1 of the present application cell further comprises an input inverter (106) connected to first switching means (103a through 104) and at least one of inputs.

Re claim 9, the admitted prior art further discloses in Figure 1 of the present application at least one of inputs is connected to second switching means (103b through 104).

Re claim 10, it is a multiplier which has a Booth encoder as cited in claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it is a multiplier which has a Booth encoder as cited in claim 2. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 12, it is a multiplier which has a Booth encoder as cited in claim 3. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 17, it is a multiplier which has a Booth encoder as cited in claim 8. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 18, it is a multiplier which has a Booth encoder as cited in claim 9. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 19, it is a multiply-accumulate module which has a Booth encoder as cited in claim 1. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 20, it is a multiply-accumulate module which has a Booth encoder as cited in claim 1. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 1. In addition, the admitted prior art further discloses in Figure 1 a critical path transistor level within Booth encoding circuit is less than ten (100).

Allowable Subject Matter

8. Claims 4-7 and 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,442,576 to Gergen et al. disclose a multibit shifting apparatus, data processor using same and method therefor.

b. U.S. Patent No. 6,125,379 to Lin discloses a parallel VLSI shift switch logic devices.

c. U.S. Patent No. 6,535,902 to Goto discloses a multiplier circuit for reducing the number of necessary elements without sacrificing high speed capability.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

August 6, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100